Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor memory having mutually crossing word and bit lines at which magnetoresistive memory cells are arranged, comprising:

a first magnetic layer having a first magnetization axis;

~~an insulating layer arranged in between; and~~

a second magnetic layer having a second magnetization axis, wherein the first magnetic layer is formed from hard ferromagnetic material, the second magnetic layer is formed from soft ferromagnetic material, and the first and the second magnetization axes intersect if projected into a plane spanned by the word ~~(8)~~ and the bit line ~~(9)~~;

an insulating layer arranged in between the first and second magnetic layers; and

a circuit arrangement for evaluating the information content of at least one of the magnetoresistive memory cells, the circuit arrangement including

an AC current source connected to the memory cell via a word line; and

a voltage measuring device measuring the voltage to the word line and to the memory cell, via a bit line, the memory cell being connected with a magnetoresistive resistance between the word and the bit line.

2. (Original) The semiconductor memory as claimed in claim 1, wherein the magnetoresistive resistance is based on the tunnel magnetoresistive effect of the combination of layer materials.

3. (Original) The semiconductor memory as claimed in claim 1, wherein the magnetoresistive resistance is based on the giant magnetoresistive effect of the combination of layer materials.

4. (Original) The semiconductor memory as claimed in claim 1, wherein the second magnetization axis of the second magnetic layer is arranged parallel to a first of the word or bit lines.

5. (Original) The semiconductor memory as claimed in claim 4, wherein the first magnetization axis of the first magnetic layer is arranged perpendicular to the second magnetization axis.

6. Canceled.

7. (Currently Amended) The semiconductor memory as claimed in ~~claim 6~~ claim 1, wherein the word line connected to the AC current source is connected to a ground potential via an additional resistance, and the resistance of the magnetoresistive memory cell has at least the magnitude of the additional resistance.

8. (Original) The semiconductor memory as claimed in claim 7, wherein the word line has an interconnect resistance, and the value of the additional resistance has at least the value of the interconnect resistance.

9. (Currently Amended) The semiconductor memory as claimed in ~~claim 6~~ claim 1, wherein the voltage measuring device has a unit for detecting a DC voltage component.

10. (Currently Amended) The semiconductor memory as claimed in claim 9, wherein the unit for detecting a DC voltage component has at least one of a low-pass filter, an amplifier, a comparator, and an integration unit.

11. (Currently Amended) The semiconductor memory as claimed in ~~claim 6~~ claim 1, wherein the voltage measuring device has a unit for the phase-selective measurement of voltage harmonics.

12. (Currently Amended) A ~~The~~ semiconductor memory ~~as claimed in claim 1~~ having mutually crossing word and bit lines at which magnetoresistive memory cells are arranged, comprising ~~, further comprising~~:

a first magnetic layer having a first magnetization axis;

a second magnetic layer having a second magnetization axis, wherein the first magnetic layer is formed from hard ferromagnetic material, the second magnetic layer is formed from soft ferromagnetic material, and the first and the second magnetization axes intersect if projected into a plane spanned by the word and the bit line;

an insulating layer arranged in between the first and second magnetic layers; and

a circuit arrangement for evaluating the information content of at least one of the magnetoresistive memory cells, the circuit arrangement ~~having~~ including an AC voltage source connected to the memory cell via a word line, and a current measuring device for measuring the current flow between the bit line and a ground potential, one memory cell being connected with a magnetoresistive resistance between the word and the bit line.

13. (Original) The semiconductor memory as claimed in claim 12, wherein the word line connected to the AC voltage source is connected to a ground potential via an additional resistance, and the magnetoresistive resistance of the memory cell has at least the magnitude of the additional resistance.

14. (Original) The semiconductor memory as claimed in claim 13, wherein the word line has an interconnect resistance, and the additional resistance has at least the value of the interconnect resistance.

15. (Original) The semiconductor memory as claimed in claim 12, wherein the current measuring device has a unit for detecting a DC current component.

16. (Original) The semiconductor memory as claimed in claim 15, wherein the unit for detecting a DC current component has at least one of a low-pass filter, an amplifier, a comparator, and an integration unit.

17. (Original) The semiconductor memory as claimed in claim 12, wherein the current measuring device has a unit for the phase-selective measurement of current flow harmonics.

18. (Currently Amended) A method for operating ~~the~~ a semiconductor memory ~~as claimed in claim 1,~~ for evaluating the information content of at least one of the magnetoresistive memory cells, the semiconductor memory having mutually crossing word and bit lines at which magnetoresistive memory cells are arranged, including a first magnetic layer having a first magnetization axis; a second magnetic layer having a second magnetization axis, wherein the first magnetic layer is formed from hard ferromagnetic material, the second magnetic layer is formed from soft ferromagnetic material, and the first and the second magnetization axes intersect if projected into a plane spanned by the word and the bit line; an insulating layer arranged in between the first and second magnetic layers; and a circuit arrangement for evaluating the information content of at least one of the magnetoresistive memory cells, the circuit arrangement including an AC voltage source connected to the memory cell via a word line, and a current measuring device for measuring the current flow between the bit line and a ground potential, one memory cell being connected with a magnetoresistive resistance between the word and the bit line, the method comprising:

feeding ~~an AC current~~ ~~or~~ an AC voltage having constant frequency and amplitude into the word line connected to the memory cell to be evaluated;

measuring a signal during a measurement duration, the signal being derived from the intensity of the current flow through the sequence of layers of the memory cell with a magnetoresistive resistance by the current measuring device; and

evaluating the information content of the memory cell depending on the profile of the signal during the measurement duration.

19. (Currently Amended) The method as claimed in claim 18, wherein the signal derived from the measurement in the current ~~or voltage~~ measuring device includes the ~~DC current or~~ DC voltage component of the measured ~~AC current or~~ AC voltage profile, and the evaluation is carried out in a manner dependent on the sign of the ~~DC current or~~ DC voltage component.

20. (Currently Amended) The method as claimed in claim 18, wherein, the signal derived from the measurement in the current ~~or voltage~~ measuring device includes the first harmonic of the ~~AC current or~~ AC voltage profile with double the ~~AC current or~~ AC voltage frequency fed in, and the evaluation is carried out in a manner dependent on the sign of the harmonic in the case of a predetermined phase.

21. (Original) The method as claimed in claim 20, wherein a phase-selective lock-in technique is used.

22. (Original) The method as claimed in claim 18, wherein the measurement duration is less than 20 nanoseconds.

23. (Currently Amended) The method as claimed in claim 18, wherein the ~~AC current or~~ AC voltage frequency is more than 100 megahertz.

24. (Currently Amended) A method for operating ~~the~~ a semiconductor memory ~~as claimed in claim 1,~~ for evaluating the information content of at least one of the magnetoresistive memory cells, the semiconductor memory having mutually crossing word and bit lines at which magnetoresistive memory cells are arranged, including a first magnetic layer having a first magnetization axis; a second magnetic layer having a second magnetization axis, wherein the first magnetic layer is formed from hard ferromagnetic material, the second magnetic layer is formed from soft ferromagnetic material, and the first and the second magnetization axes intersect if projected into a plane spanned by the word and the bit line; an insulating layer arranged in between the first and second magnetic layers; and a circuit arrangement for evaluating the information content of at least one of the magnetoresistive memory cells, the circuit arrangement including an AC current source connected to the memory cell via a word line, and a voltage measuring device for measuring the voltage to the word line and to the memory cell, via a bit line, the memory cell being connected with a magnetoresistive resistance between the word and the bit line, the method comprising:

feeding an AC current ~~or an AC voltage~~ having constant frequency and amplitude into the word line connected to the memory cell to be evaluated;

measuring a signal during a measurement duration, the signal being derived from the voltage between the bit and the word line by the voltage measuring device; and

evaluating the information content of the memory cell depending on the profile of the signal during the measurement duration.

25. (Currently Amended) The method as claimed in claim 24, wherein the signal derived from the measurement in the ~~current or~~ voltage measuring device includes the DC current ~~or DC voltage~~ component of the measured AC current ~~or AC voltage~~ profile, and the evaluation is carried out in a manner dependent on the sign of the DC current ~~or DC voltage~~ component.

26. (Currently Amended) The method as claimed in claim 24, wherein the signal derived from the measurement in the ~~current or~~ voltage measuring device includes the first harmonic of the AC current ~~or AC voltage~~ profile with double the AC current ~~or AC voltage~~ frequency fed in, and the evaluation is carried out in a manner dependent on the sign of the harmonic in the case of a predetermined phase.

27. (Original) The method as claimed in claim 26, wherein a phase-selective lock-in technique is used.

28. (Original) The method as claimed in claim 24, wherein the measurement duration is less than 20 nanoseconds.

29. (Currently Amended) The method as claimed in claim 24, wherein the AC current ~~or AC voltage~~ frequency is more than 100 megahertz.

30. (New) The semiconductor memory as claimed in claim 12, wherein the magnetoresistive resistance is based on the tunnel magnetoresistive effect of the combination of layer materials.

31. (New) The semiconductor memory as claimed in claim 12, wherein the magnetoresistive resistance is based on the giant magnetoresistive effect of the combination of layer materials.

32. (New) The semiconductor memory as claimed in claim 12, wherein the second magnetization axis of the second magnetic layer is arranged parallel to a first of the word or bit lines.

33. (New) The semiconductor memory as claimed in claim 32, wherein the first magnetization axis of the first magnetic layer is arranged perpendicular to the second magnetization axis.